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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,711	10/18/2000	Jens Wildhagen	450117-02749	4972

20999 7590 11/01/2005

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,711	WILDHAGEN, JENS	
	Examiner	Art Unit	
	Khanh Tran	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 20-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 21-25* is/are rejected.

7)☒ Claim(s) *4-9 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Request For Continued Examination (RCE) filed on 10/07/2005 has been entered. Claims 1-9 and 20-25 are pending in this Office action.

Response to Arguments

2. Applicant's arguments filed on 03/23/2005 have been fully considered but they are not persuasive. A full explanation is discussed in the following claim rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Reich U.S. Patent 4,827,515.

Regarding claim 1, Reich invention is directed to a digital demodulator for demodulating and separating the individual components of a digitized stereo multiplex signal (MPX). Hence, the digital demodulator corresponds to the claimed stereo demultiplexer in the preamble.

As shown in figure 1, the digital demodulator, receiving a digitized composite signal sx, outputs a stereo sum signal ss, a pilot signal ps, and a stereo difference signal df. In view of the foregoing disclosure, the digitized composite signal sx corresponds to the claimed frequency demodulated stereo-multiplex signal, see also figure 2. The digitized composite MPX signal sx includes a stereo sum signal ss, a pilot signal ps, and a stereo difference signal df as claimed in the application claim.

In column 4 lines 40-59, see also figure 1, Reich teaches that the quadrature component pv of the pilot signal ps, which component was transformed down to zero, is amplified by an amplifier v and then applied as a control signal st to a variable frequency and phase oscillator vo. The variable oscillator vo is part of a phase-locked loop which is completed via the carrier conditioning circuit tr, one of the five carriers t1-t5 with the respective associated low-pass filter b1-b4, b6, and the control signal st. In view of the foregoing teachings, ***the digital demodulator as illustrated in figure 1 includes a phase-locked loop*** in the form of a variable oscillator vo, the carrier conditioning circuit tr, one of the five carriers t1-t5 with the respective associated low-pass filter b1-b4, b6, and the control signal st.

In column 2, line 40-50, see also figure 1, Reich teaches that the signal frequency fs, i.e. the fundamental frequency of the first and second carriers t1, t2, is equal to the pilot signal frequency fp, 19 kHz. In view of the foregoing

disclosure, the PLL as taught by Reich is configured to recover a pilot signal, which corresponds to the claimed pilot carrier.

In column 3 lines 60-68, Reich teaches that the output of the second decimation circuit d2, namely ds', containing the decimated stereo sum signal ss and the pilot signal ps, is inputted to the phase-locked loop as described above. In view of that, the second decimated composite signal ds' corresponds to the claimed "*input signal*". Furthermore, referring to figure 1, the second decimated composite signal ds' is first sampling rate decimated by decimation circuit d1 by a decimation factor M, which corresponds to the claimed "decimation factor of D". The second decimated composite signal ds' is first sampling rate decimated with regard to the digitized composite signal sx.

In addressing Applicant's arguments (pages 7-8) that "Reich does not teach or suggest the claim feature of independent claims 1 and 3, wherein the input signal, in essence, solely comprises the stereo-sum signal and the pilot signal".

The Examiner responses that the arguments are not persuasive for the following reasons: Applicant correctly points out that Reich teachings of the signal ds' contains the stereo-sum signal ss and the pilot signal ps and that the pilot signal ps contains, as interfering signals, the un-modulated stereo-difference signal df*. However, the manner of operating the device does not differentiate apparatus claim from the prior art. Referring back to figure 1 in Reich invention,

the digital demodulator as illustrated in figure 1 includes a phase-locked loop in the form of a variable oscillator vo, the carrier conditioning circuit tr, one of the five carriers t1-t5 with the respective associated low-pass filter b1-b4, b6, and the control signal st. Since Reich teachings meet all the claimed limitations, the application claim is rejected as being anticipated by Reich teachings.

A claim containing a "recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus" if the prior art apparatus teaches all the structural limitations of the claim. *Ex parte Masham,* 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987), see also MPEP 2114.

Conclusion: For the aforementioned reasons, claim 1 still stands rejected by Reich teachings.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-3 and 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Reich U.S. Patent 4,827,515.

Regarding claim 2, referring back to figure 1, Reich does not expressly teach the sampling rate decimated stereo-sum signal ss is further sampling rate decimated by a decimation factor of E before the PLL circuit receives it as input signal as claimed in the application claim. In column 2, lines 5-20, the first decimation circuit d1 is a first decimated composite signal ds, which is applied to a second decimation circuit d2 to produce a second decimated composite signal ds' containing the stereo sum signal ss and the pilot signal ps. Because the second decimated composite signal ds' contains the stereo sum signal ss, one of ordinary skill in the art at the time of the invention would have recognized that the stereo sum signal ss is further sampling rate decimated by a factor of 3, which corresponds to the claimed a decimation factor of E before the PLL circuit receives the second decimated composite signal ds' as input signal. Motivation is the decimated composite signal ds including the stereo sum signal ss. In view of that, the stereo sum signal ss is first decimated by the decimation circuit d1.

Regarding claim 3, claim 3 is rejected on the same ground as for claim 1 because of similar scope. Furthermore, Reich does not show a recovered pilot carrier, which is interpolated so that it has a sampling rate equal to that of the frequency demodulated stereo-multiplex signal.

Referring back to figure 1, in column 2, lines 10-30, Reich teaches that the first decimation circuit d1 is a first decimated composite signal ds. The decimated composite signal ds is still the digitized standard stereo multiplex standard, but at different sampling rate. In view that, the decimated composite stereo signal ds

corresponds to the claimed frequency demodulated stereo-multiplex signal (m(t)). Furthermore, the output carrier t3 of the phase-locked loop, used to demodulate the stereo difference signal df, has a sampling rate substantially equal to that of the decimated standard stereo multiplex signal ds. First, t3 is derived from the pilot signal ps, which is derived from the signal ds'. The signal ds' is decimated by a decimator d2. From figure 1, because the signal ds' and the pilot signal ps have lower sampling rate than that of the input to m3 (see figure 1), it would have been obvious for one of ordinary skill in the art at the time the invention was made that the recovered carrier t3 can be modified to be interpolated in order to have the same sampling rate as the decimated stereo composite signal ds. The motivation is that the carrier t3 must have the same sampling rate as that of the decimated stereo multiplex signal ds since the sampling rate of both signals must be the same in order to demodulate the stereo difference signal df from the decimated standard stereo multiplex signal ds.

Regarding claim 21, *in response to Applicant's arguments on page 8, the Examiner responses with the new rejection*. Regarding claim 21 is rejected on the same ground as for claim 2 because of similar scope. Furthermore, referring to figure 1, the two signals fed to decimation circuit d2 and mixer m3 are intermediate signals, corresponding to the claimed "first and second intermediate signals". The decimation

circuit d2, corresponding to the claimed "sampling rate decimator", is configured and adapted for sampling rate decimating one of the intermediate signals.

Regarding claim 22, as recited in claim 21, the standard MPX signal, the amplitudes of the stereo sum signal ss and the demodulated stereo difference signal df are chosen that, by forming the sum or the difference of these signals as is commonly done in stereo decoders, for example, the left and right signals are obtained directly. In light of the foregoing, an adder can be implemented to form the sum or the difference of these signals.

Regarding claim 23, claim 23 is rejected on the same ground as for claim 21 because of similar scope. Furthermore, the second decimated composite signal ds' and the output of the decimation circuit d3 correspond to the claimed "first and second intermediate signals". The second decimated composite signal ds' corresponds to the claimed "the input signal".

Regarding claim 24, claim 24 is rejected on the same ground as for claim 22 because of similar scope.

Regarding claim 25, referring back to figure 1, in column 2, lines 10-30, Reich teaches that the first decimation circuit d1 is a first decimated composite signal ds. The decimated composite signal ds is still the digitized standard stereo multiplex standard sx, but at different sampling rate. Furthermore, the output carrier t3 of the phase-locked

loop, used to demodulate the stereo difference signal df, has a sampling rate substantially equal to that of the decimated standard stereo multiplex signal ds. First, t3 is derived from the pilot signal ps, which is derived from the signal ds'. The signal ds' is decimated by a decimator d2. From figure 1, because the signal ds' and the pilot signal ps have lower sampling rate than that of the input to m3 (see figure 1), it would have been obvious for one of ordinary skill in the art at the time the invention was made that the recovered carrier t3 can be modified to be interpolated in order to have the same sampling rate as the decimated stereo composite signal ds. The motivation is that the carrier t3 must have the same sampling rate as that of the decimated stereo multiplex signal ds since the sampling rate of both signals must be the same in order to demodulate the stereo difference signal df from the decimated standard stereo multiplex signal ds.

Allowable Subject Matter

5. Claims 4-9 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh cong Tran 10/28/2005

Examiner KHANH TRAN